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METHOD AND APPARATUS FOR CONTROLLING HEAD VELOCITY IN A DISK DRIVE DURING RAMP LOAD/UNLOAD

FIELD OF THE INVENTION

The present invention relates to controlling head velocity in a disk drive during ramp load or unload.

BACKGROUND OF THE INVENTION

Disk drives include one or more disks on which digital information is stored as magnetic charges. The disk (or disks) is mounted on a spindle rotated by a spindle motor. An actuator assembly includes an actuator arm and a voice coil motor (VCM). The actuator arm extends from the VCM and supports a slider that includes a read/write head. The head reads from and writes to the disk as the slider flies over the disk on an air cushion. The VCM positions the head at desired locations relative to the disk.

Disk drives have been designed with a landing zone at the inner diameter of the disk to park the head. The landing zone is a takeoff or landing spot for the head as the disk starts or stops spinning, respectively. As the disk starts spinning, the head is dragged on the disk until the disk reaches a speed that creates sufficient air pressure for the head to separate from and fly over the disk.

The disk can have a rough texture to minimize friction between the head and the disk in the landing zone. However, as disk drive storage capacity increases, the flying height of the head decreases, and the disk is given a smooth texture to avoid damaging the head. The smooth texture dramatically increases the contact friction between the head and the disk in the landing zone. As a

result, increased spindle motor current may be required to break the head loose from the disk to allow the disk to rotate, or spin up.

Disk drives have increasingly smaller form factors, or disk sizes (2.5", 1.8" and 1"). Small form factors are useful in battery-operated devices where increased spindle motor current to spin up the disk is undesirable. Small form factors reduce the disk surface area, which is reduced further by a landing zone. Small form factors are also more susceptible to operational and non-operational shock if the head and the disk are in contact. Thus, small form factors are penalized by a landing zone.

Disk drives have been designed with a ramp to avoid a landing zone. The head is lifted off the disk and unloaded on the ramp while the disk is spinning, and then the disk decelerates and stops spinning. When power is reapplied to the spindle motor, the disk spins up, and once the disk has sufficient speed for the head to fly, the head is loaded from the ramp and positioned over the disk.

During ramp load/unload, the head velocity is accurately controlled to avoid damaging the head or the disk at a contact point. As the VCM moves through its magnetic poles, it generates a back electromotive field (EMF) voltage which is proportional to its speed. The back EMF voltage also indicates the head velocity. The back EMF voltage (Vbemf) can be calculated based on the total voltage across the VCM (Vvcm) and the IR drop across the VCM (Ivcm x Rvcm) as follows:

$$Vbemf = Vvcm - (Ivcm \; x \; Rvcm) \qquad (1)$$

Thus, the back EMF voltage is measured by removing the VCM IR drop from the VCM voltage.

The back EMF voltage can be measured by a pulse width modulation (PWM) technique or an IR cancellation technique. In the PWM technique, the VCM is turned off periodically, forcing the VCM current to zero. Since the IR drop across the VCM is zero, the back EMF voltage is readily measured. In the IR cancellation technique, the back EMF voltage is determined by measuring the gain of a servo loop. Since the VCM current is not periodically turned off,

calibrations cancel the IR drop from the VCM voltage. The calibrations may need to be repeated because temperature and voltage deviations cause the gain of the servo loop to change frequently over time.

The PWM technique requires less hardware and fewer calibrations than the IR cancellation technique. However, the PWM technique may generate audible noise during ramp load/unload. The IR cancellation technique, however, requires robust calibration with more hardware. Further, increased voltage resolution may require a hardware change to increase the number of bits of the analog-to-digital converter.

Disk drives have been designed for either the PWM or IR cancellation techniques. If both techniques were needed, two distinct sets of hardware had to be implemented, thereby increasing cost. Further, the technique needed to be selected before any voltage measurements, thereby greatly reducing flexibility.

There is, therefore, a need for a disk drive with accurate control of the head during ramp load/unload. There is also a need for a disk drive that measures the back EMF voltage with either the PWM technique or the IR cancellation technique without hardwiring a specific measurement technique or making multiple calibrations prior to operation of the disk drive.

SUMMARY OF THE INVENTION

To achieve these and other advantages and in accordance with the present invention, as embodied and broadly described, a method and apparatus for controlling the velocity of a head during a ramp load/unload are disclosed.

A disk drive controls head velocity during ramp load/unload by measuring voltages across a VCM and a sense resistor in series with the VCM, calculating a back EMF voltage using the VCM and sense resistor voltages, and adjusting the head velocity using the back EMF voltage.

An embodiment includes amplifying the VCM and sense resistor voltages, multiplexing the amplified voltages, digitizing the multiplexed voltages and calculating the back EMF voltage in discrete-time based on the digitized voltages.

Another embodiment includes selecting between the PWM and IR cancellation techniques and calculating the back EMF voltage using the selected technique without two distinct sets of hardware.

Another embodiment includes calculating a calibration constant by comparing reference voltages across the VCM and the sense resistor while no current is applied to the VCM with voltages across the VCM and the sense resistor while current is applied to the VCM.

Another embodiment includes calculating a control variable in the discrete time domain using a proportional-integral control technique that compares a target head velocity to an actual head velocity and adjusting the head velocity based on the control variable.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the present invention are more fully described in the following drawings and accompanying text in which like reference numbers represent corresponding elements throughout:

FIG. 1 illustrates a disk drive;

FIG. 2 illustrates ramp load/unload;

FIG. 3 illustrates a ramp load/unload control circuit;

FIG. 4 is a flowchart of a calibration algorithm; and

FIG. 5 is a flowchart of a load/unload algorithm; and

FIG. 6 is a flowchart of a velocity compensation algorithm.

DETAILED DESCRIPTION

FIG. 1 illustrates a conventional disk drive 100 that includes a voice coil motor (VCM) 105, a disk 110, a cover 115, an actuator arm 120, a spindle 125, a

DC power input 130, a read/write head 135, a base casting 140, an I/O connector 145, a printed circuit board 150, a frame/bracket 155, a connector 160, a printed circuit cable 165 and a shock mount 170.

The disk 110 is coated on both sides with media that stores information. The disk 110 is mounted on the cylindrical spindle 125 that, during operation, rotates the disk 110 at high speed. The head 135 is positioned over and reads from and writes to the disk 110. The head 135 is embedded in a slider mounted on the actuator arm 120. The VCM 105 and the actuator arm 120 form an actuator assembly that moves the head 135 relative to the disk 110 as needed for read/write operations. The disk drive 100 is enclosed by the cover 115 and the base casting 140.

FIG. 2 illustrates ramp load/unload in the disk drive 100. The disk drive 100 includes a ramp 175, and the actuator arm 120 includes a lift tab 180. During read/write operations, the head 135 flies over the disk 110 at a read/write position 185 on an air cushion caused by the rotation of the disk 110. During ramp unload, the VCM 105 moves the head 135 from the disk 110 onto the ramp 175 while the disk 110 is still spinning. After the head 135 comes to rest at a park position 190, the disk drive 100 stops the rotation of the disk 110. Similarly, during ramp load, the disk drive 100 spins up the disk 110, and when the disk 110 spins at sufficient velocity for the head 135 to fly above the disk 110, the VCM 105 moves the head 135 from the ramp 175 to the disk 110.

FIG. 3 illustrates a ramp load/unload control circuit 300. The control circuit 300 includes a driver 305, a first operational amplifier 310, a second operational amplifier 315, a multiplexer 320, an analog-to-digital converter (ADC) 325 and a microprocessor 330.

The VCM 105 has an internal resistance (Rvcm) 105A, a back EMF voltage (Vbemf) 105B and a total voltage (Vvcm). The VCM 105 is connected in series with a sense resistor 195 with a sense resistance (Rsense).

The driver 305 has a first output that is connected to the VCM 105 and a positive input of the first operational amplifier 310, and a second output that is

connected to the sense resistor 195 and a negative input of the second operational amplifier 315. The VCM 105 is connected to the sense resistor 195, a negative input of the first operational amplifier 310 and a positive input of the second operational amplifier 315 at a node.

The driver 305 powers the VCM 105 by sending a current through the VCM 105 and the sense resistor 195. The first operational amplifier 310 receives and amplifies the total voltage across the VCM 105 (Vvcm). The second operational amplifier 315 receives and amplifies the voltage across the sense resistor 195 (Vrsense). The multiplexer 320 selects between the amplified VCM voltage from the first operational amplifier 310 at a first voltage path and the amplified sense resistor voltage from the second operational amplifier 315 at a second voltage path in response to a sample signal from the microprocessor 330. The ADC 325 coverts the multiplexed voltage selected by the multiplexer 320 from analog to digital format, and sends the digital signal along a serial port to the microprocessor 330.

The microprocessor 330 calculates the back EMF voltage based on the VCM voltage and the sense resistor voltage, as amplified by the operational amplifiers 310 and 315, multiplexed by the multiplexer 320 and digitized by the ADC 325. The microprocessor 330 also calculates the VCM velocity based on the back EMF voltage, and sends a control signal to the driver 105 in a feedback loop to accurately control the head velocity.

The microprocessor 330 calculates the back EMF voltage by selecting between the PWM technique and the IR cancellation technique. As a result, the disk drive 100 calculates the back EMF voltage using a selected one of the PWM technique and the IR cancellation technique without implementing two distinct sets of hardware.

The microprocessor 330 calibrates the control circuit 300 using the calibration algorithm 400 described below. The calibration algorithm 400 calculates a gain calibration constant (Kcal) using the following IR cancellation technique:

$$Kcal = \frac{i \times Rvcm \times Kvcm}{i \times Rsense \times Ksense} \tag{2}$$

if $Kvcm = 1$ and $Ksense = 1$ then

$$Kcal = \frac{i \times Rvcm}{i \times Rsense} \tag{3}$$

At start-up, a small VCM current is applied towards the outer crash stop making the back EMF voltage zero:

$$i \times Rvcm = Vvcm - Vref1 \tag{4}$$

$$i \times Rsense = Vrsense - Vref2 \tag{5}$$

Therefore, the following relationship is established:

$$i \times Rvcm = Kcal \times (i \times Rsense) \tag{6}$$

Substitution yields the following equality:

$$(Vvcm - Vref1) = Kcal \times (Vrsense - Vref2) \tag{7}$$

The microprocessor 330 calibrates the control circuit 300 by determining the calibration constant (Kcal) as follows:

$$Kcal = \frac{Vvcm - Vref1}{Vrsense - Vref2} \tag{8}$$

After calibrating the control circuit 300, the microprocessor 330 monitors the back EMF voltage at sample times to determine whether to increase or decrease the current controlling the head velocity.

Figure 4 is a flow chart of a calibration algorithm 400 that the control circuit 300 implements to determine a gain calibration constant (Kcal) at power-up of the disk drive 100. At step 405, the calibration algorithm 400 starts. At step 410, the driver 305 turns off the current to the VCM 105. At step 415, the microprocessor 330 measures the VCM voltage (Vvcm) and the sense resistor voltage (Vrsense) to provide a first reference voltage (Vref1) and a second reference voltage (Vref2) respectively. At step 420, the driver 305 applies a small current to the VCM 105 to urge the head 135 in the unload direction (towards a crash stop, away from the disk 110). At step 425, the multiplexer 320 selects the

VCM voltage (Vvcm), and at step 430, the multiplexer 320 selects the sense resistor voltage (Vrsense). At step 435, the microprocessor 330 calculates the calibration constant (Kcal) according to equation (8). At step 440, the calibration algorithm 400 ends.

Figure 5 is a flow chart of a load/unload algorithm 500 that the control circuit 300 implements to control the velocity of the head 135 during ramp load/unload. At step 505, the load/unload algorithm starts. At step 510, the microprocessor 330 determines whether the head 135 is being loaded from or unloaded onto the ramp 175. If the head 135 is being loaded from the ramp 175, then at step 515 the microprocessor 330 sets the voltage corresponding to the target velocity of the head 135 (Vloadtarget). At step 520, the microprocessor 330 measures the VCM voltage (Vvcm) and the sense resistor voltage (Vrsense). At step 525, the microprocessor 330 calculates the back EMF voltage (Vbemf) as follows:

$$Vbemf = (Vvcm - Vref1) - Kcal \times (Vrsense - Vref2) \quad (9)$$

At step 530, the microprocessor 330 calculates a velocity error (Verr) as follows:

$$Verr = Vloadtarget - Vbemf \quad (10)$$

At step 535, the microprocessor 330 performs the velocity compensation algorithm 600 described below to adjust the velocity of the head 135. At step 540, the microprocessor 330 determines whether the head 135 is loaded on the disk 110. If the loading procedure is not complete, then at step 545 the microprocessor 330 waits for the next sampling period and then the process returns to step 520 to measure the next VCM voltage (Vvcm) and sense resistor voltage (Vrsense). If the loading procedure is complete, then at step 550 the head 135 is locked into tracking mode and at step 595 the load/unload algorithm 500 ends.

Returning to step 510, if the microprocessor 330 determines that the head 135 is being unloaded onto the ramp 175, then at step 555 the microprocessor 330

sets the voltage corresponding to the target velocity of the head 135 (Vunloadtarget). At step 560, the microprocessor 330 measures the VCM voltage (Vvcm) and the sense resistor voltage (Vrsense). At step 565, the microprocessor 330 calculates the back EMF voltage (Vbemf) according to equation (9). At step 570 the microprocessor 330 calculates the velocity error (Verr) as follows:

$$Verr = Vunloadtarget - Vbemf \quad (11)$$

At step 575, the microprocessor 330 performs the velocity compensation algorithm 600 described below to adjust the velocity of the head 135. At step 580, the microprocessor 330 determines whether the head is unloaded from the disk 110. If the unloading procedure is not complete, then at step 585 the microprocessor 330 waits for the next sampling period and then the process returns to step 560 to measure the next VCM voltage (Vvcm) and sense resistor voltage (Vrsense). If the unloading procedure is complete, then at step 590 the VCM 105 is disabled and at step 595 the load/unload algorithm 500 ends.

Figure 6 is a flow chart of a velocity compensation algorithm 600 that the microprocessor 330 initiates to correct the velocity of the head 135. At step 605, the velocity compensation algorithm 600 begins. At step 610, the microprocessor 330 determines the velocity error (Verr(n)) for the current sample as previously described in steps 530 or 570 of the load/unload algorithm 500. At step 615, the microprocessor 330 determines a discrete control variable (control(n)) that will be used by the driver 305 to adjust the head velocity. Although several methods of velocity compensation are well known in the art and may be employed in the present invention, the preferred embodiment employs a proportional-integral control technique, where Kp is a proportional constant and Ki an integral constant. Both Kp and Ki are selected according to the desired frequency and transient responses for the velocity control loop. The proportional-integral control technique calculates the discrete control variable in the continuous time domain as follows:

$$Output\_command = \left(Kp + \frac{Ki}{S}\right) \times Verr \quad (12)$$

The microprocessor 330 calculates the discrete control variable (control(n)) in the discrete time domain using the proportional-integral control technique as follows:

$$Control(n) = Control(n-1) + Ki \times (T - Kp) \times Verr(n-1) + Kp \times (Verr(n)) \quad (13)$$

where (n) denotes the current sample and (n–1) denotes the previous sample. The discrete control variable corrects the head velocity by comparing the voltage corresponding to the target velocity with the voltage corresponding to the actual velocity of the head 135 as determined by the back EMF voltage. At step 620, the microprocessor 330 sends the discrete control variable to the driver 305, and the driver 305 adjusts the head velocity based on the discrete control variable. At step 625, the microprocessor 330 sets the discrete control variable and the velocity error of the current sample (control(n) and Verr(n)) to the previous sample (control(n–1) and Verr(n–1)) for use by the next sample. At step 630, the microprocessor 330 determines whether the velocity compensation algorithm 600 continues. If so, then the process returns to step 610 for the next sample, otherwise at step 635 the velocity compensation algorithm 600 ends.

EXAMPLE

The present invention is illustrated by the following example. The VCM resistance and the sense resistor are as follows:

Rvcm 320 = 17.1 Ω

Rsense 330 = 1 Ω

The gains of the first operational amplifier 310 (Kvcm) and the second operational amplifier 315 (Krsense) are as follows:

Kvcm = 5

Krsense = 4

The ADC 325 uses 12-bits with a full-scale voltage of 5 volts and has the following resolution:

$$ADC\_resolution = \frac{ADC\_FS\_voltage}{2^{ADC\_bits} - 1} = \frac{5}{2^{12} - 1} = 1.221.10^{-3}\ \text{V/count}$$

The driver 305 provides a reference voltage of 2.5 volts to the sense resistor 195 and the second operational amplifier 315 when the back EMF voltage is zero. The first and second reference voltages (Vref1 and Vref2) are as follows:

$$Vref1 = 2.520 \text{ volts}$$

$$Vref2 = 2.510 \text{ volts}$$

The ADC counts corresponding to the first and second reference voltages at the first and second voltage paths are as follows:

$$ADC\_Vref1\_count = \frac{Vref1.2^{ADC\_bits}}{ADC\_FS\_voltage} = 2064$$

$$ADC\_Vref2\_count = \frac{Vref2.2^{ADC\_bits}}{ADC\_FS\_voltage} = 2056$$

The VCM voltage (Vvcm) when the VCM current (Ivcm) is 10 mA is as follows:

$$Vvcm = Vref1 + Ivcm \times Rvcm \times Kvcm$$

$$= 2.52 \text{ v} + 10 \text{ mA x } 17.1\ \Omega \text{ x } 5$$

$$= 3.375 \text{ volts}$$

The ADC count corresponding to Vvcm is as follows:

$$ADC\_Vvcm\_count = Integer\left(\frac{Vvcm.2^{ADC\_bits}}{ADC\_FS\_voltage} - ADC\_Vref1\_count\right)$$

$$= (3.375 \text{ v x } 4096) / 5\text{v} - 2064$$

$$= 701$$

The Vrsense is as follows:

$$Vrsense = Vref2 + Ivcm \times Rsense \times Ksense$$

$$= 2.51 + 10 \text{ mA x } 1\ \Omega \text{ x } 4$$

$$= 2.55 \text{ volts}$$

The ADC count corresponding to Vrsense is as follows:

$$ADC\_Vrsense\_count = Integer\left(\frac{Vrsense.2^{ADC\_bits}}{ADC\_FS\_voltage} - ADC\_Vref2\_count\right)$$

$$= (2.55\ v \times 4096) / 5v - 2056$$

$$= 33$$

Finally, the calibration constant (Kcal) is as follows:

$$Kcal = \frac{ADC\_Vvcm\_count}{ADC\_Vrsense\_count}$$

$$= 700 / 33$$

$$= 21.21$$

The number of bits in the ADC 325 may be increased if greater accuracy or resolution is desired, or reduced to decrease computational burden.

It will be apparent to those skilled in the art that various modifications and variations can be made to the embodiments described above without departing from the spirit or the scope of the invention. Thus, it is intended that the present invention cover modifications and variations that come within the claims and their equivalents.